Note: National Semiconductor recommends replacing 2N2920 and 2N3728 matched pairs with LM394 in all application circuits.

Section 1—Basic Circuits

Inverting Amplifier

\[ V_{OUT} = -\frac{R_2}{R_1} V_{IN} \]

\[ R_{IN} = R_1 \]

Non-Inverting Amplifier

\[ V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN} \]

Difference Amplifier

\[ V_{OUT} = \frac{R_1 + R_2}{R_3 + R_4} \left( \frac{R_4}{R_1} V_2 - \frac{R_2}{R_1} V_1 \right) \]

For R1 = R3 and R2 = R4

\[ V_{OUT} = \frac{R_2}{R_1} (V_2 - V_1) \]

\[ R_1//R_2 = R_3//R_4 \]

Inverting Summing Amplifier

\[ V_{OUT} = -\left( \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) \]

\[ R_5 = R_1//R_2//R_3//R_4 \]

For minimum offset error due to input bias current
Section 1—Basic Circuits (Continued)

Non-Inverting Summing Amplifier

Inverting Amplifier with High Input Impedance

*\( R_S = 1k \) for 1% accuracy

Source Impedance less than 100k gives less than 1% gain error.

Fast Inverting Amplifier with High Input Impedance

Non-Inverting AC Amplifier

\[ V_{OUT} = \frac{R_1 + R_2}{R_1} \cdot V_{IN} \]

\[ R_{IN} = R_3 \]

\[ R_3 = \frac{R_1}{R_2} \]
Section 1—Basic Circuits (Continued)

**Practical Differentiator**

\[ f_c = \frac{1}{2\pi R_2 C_1} \]
\[ f_h = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_2 C_2} \]
\[ f_c < f_h < f_{\text{unity gain}} \]

**Integrator**

\[ V_{\text{OUT}} = -\frac{1}{R_1 C_1} \int_{t_0}^{t_1} V_{\text{IN}} \, dt \]
\[ f_c = \frac{1}{2\pi R_1 C_1} \]
\[ R_1 = R_2 \]

For minimum offset error due to input bias current

**Fast Integrator**

**Current to Voltage Converter**

\[ V_{\text{OUT}} = \ln R_1 \]

*For minimum error due to bias current \( R_2 = R_1 \)*
Section 1—Basic Circuits

Circuit for Operating the LM101 without a Negative Supply

Neutralizing Input Capacitance to Optimize Response Time

Integrator with Bias Current Compensation

Circuit for Generating the Second Positive Voltage

Voltage Comparator for Driving DTL or TTL Integrated Circuits

Threshold Detector for Photodiodes

*Adjust for zero integrator drift.
Current drift typically 0.1 nA/°C over −55°C to 125°C temperature range.
Section 1—Basic Circuits

Double-Ended Limit Detector

\[ V_{OUT} = 4.6V \text{ for } V_{LT} \leq V_{IN} \leq V_{UT} \]
\[ V_{OUT} = 0V \text{ for } V_{IN} < V_{LT} \text{ or } V_{IN} > V_{UT} \]

Multiple Aperture Window Discriminator

\[ V_{IN} > V_{4} \]
\[ V_{3} < V_{IN} < V_{4} \]
\[ V_{2} < V_{IN} < V_{3} \]
\[ V_{1} > V_{I} \]
Section 1—Basic Circuits (Continued)

Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element

\[
\text{RANGE} = \pm V \left( \frac{R_2}{R_1} \right)
\]

Offset Voltage Adjustment for Non-Inverting Amplifiers Using Any Type of Feedback Element

\[
\text{RANGE} = \pm V \left( \frac{R_2}{R_1} \right)
\]

\[
\text{GAIN} = 1 + \frac{R_5}{R_4 + R_2}
\]

Offset Voltage Adjustment for Voltage Followers

\[
\text{RANGE} = \pm V \left( \frac{R_3}{R_1} \right)
\]

Offset Voltage Adjustment for Differential Amplifiers

\[
\text{RANGE} = \pm V \left( \frac{R_5}{R_4} \left( \frac{R_1}{R_1 + R_3} \right) \right)
\]

\[
\text{GAIN} = \frac{R_2}{R_1}
\]
Section 1—Basic Circuits  (Continued)

Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less

\[ R_1 = 2000 \frac{R_3}{R_4} \]
\[ R_4/R_3 \leq 10 \text{k}\Omega \]
\[ \text{RANGE} = \pm V \left( \frac{R_3/R_4}{R_1} \right) \]

Section 2 — Signal Generation

Low Frequency Sine Wave Generator with Quadrature Output

\[ f_0 = 1 \text{ Hz} \]

\[ R_2 = 22 \text{M} \Omega \]
\[ D_1 = 6.3 \text{V} \]
\[ D_2 = 5.3 \text{V} \]

\[ C_2 = 0.02 \mu\text{F} \]
\[ C_3 = 0.01 \mu\text{F} \]
\[ C_4 = 30 \text{pF} \]
\[ C_5 = 30 \text{pF} \]
Section 2 — Signal Generation (Continued)

High Frequency Sine Wave Generator with Quadrature Output

Free-Running Multivibrator

Wein Bridge Sine Wave Oscillator

*Chosen for oscillation at 100 Hz

Eldema 1869 10V, 14 mA Bulb
Section 2 — Signal Generation  (Continued)

**Function Generator**

```
   V  
  +   LM101A  +  FREQ  +  LM107  +  Triangle Wave  +
  |  
  |  R3  140K  |  R4  1.4K  |  R5  8.2K  |
  |  
  +   R1  10K  |  R2  1M    |

Square Wave Output

C1  0.1 \(\mu\)F
```

**Pulse Width Modulator**

```
   V IN  v  
  +  +  LM101A  +  V OUT  +
  |  |  C1  0.47 \(\mu\)F  |  |
  |  |  R1  100K  |  R2  100K  |  |
  |  |  R3  100\(\Omega\)  |  R4  100K  |  |

D1  6.2V  D2  6.2V
```
Section 2 — Signal Generation

Bilateral Current Source

\[ I_{OUT} = \frac{R3 \cdot V\text{IN}}{R1 \cdot R5} \]

- \( R3 = R4 + R5 \)
- \( R1 = R2 \)

Bilateral Current Source

\[ I_{OUT} = \frac{R3 \cdot V\text{IN}}{R1 \cdot R5} \]

- \( R3 = R4 + R5 \)
- \( R1 = R2 \)
Wein Bridge Oscillator with FET Amplitude Stabilization

\[
R_1 = R_2 \\
C_1 = C_2 \\
f = \frac{1}{2\pi R_1 C_1}
\]
Section 2 — Signal Generation (Continued)

Low Power Supply forIntegrated Circuit Testing

\[ V_{OUT} = 1V/\Omega \]

**Positive Voltage Reference**

[Diagram of positive voltage reference circuit]

**Positive Voltage Reference**

[Diagram of positive voltage reference circuit]
Section 2 — Signal Generation (Continued)

Negative Voltage Reference

![Negative Voltage Reference Circuit Diagram](image)

Precision Current Sink

![Precision Current Sink Circuit Diagram](image)

Precision Current Source

![Precision Current Source Circuit Diagram](image)

\[ I_0 = \frac{V_{IN}}{R_1} \]
\[ V_{IN} \geq 0V \]
Section 3 — Signal Processing

Differential-Input Instrumentation Amplifier

![Circuit Diagram]

**Gain adjust**

\[ A_v = 10^{-6} R_6 \]
Matching determines common mode rejection.

R1 = R5 = 10R2
R2 = R3
R3 = R4
R1 = R6 = 10R3

\[ AV = \frac{R7}{R6} \]
Section 3 — Signal Processing  (Continued)

Instrumentation Amplifier with ±10 Volt Common Mode Range

R1 = R4
R2 = R5
R6 = R7
† Matching Determines CMRR

\[ \text{Av} = \frac{R6}{R2} \left( 1 + \frac{2R1}{R3} \right) \]

High Input Impedance Instrumentation Amplifier

R1 = R4; R2 = R3

\[ \text{Av} = 1 + \frac{R1}{R2} \]

†† Matching Determines CMRR
†‡ May be deleted to maximize bandwidth
Section 3 — Signal Processing  (Continued)

Bridge Amplifier with Low Noise Compensation

*Reduces feed through of power supply noise by 20 dB and makes supply bypassing unnecessary.
†Trim for best common mode rejection
‡Gain adjust

Bridge Amplifier

Precision Diode

Precision Clamp

Fast Half Wave Rectifier

*E_{REF} must have a source impedance of less than 200Ω if D2 is used.
Section 3 — Signal Processing  (Continued)

**Precision AC to DC Converter**

![Precision AC to DC Converter Diagram]

*Feedforward compensation can be used to make a fast full wave rectifier without a filter.

**Low Drift Peak Detector**

![Low Drift Peak Detector Diagram]
Section 3 — Signal Processing (Continued)

Absolute Value Amplifier with Polarity Detector

\[ V_{OUT} = -|V_{IN}| \times \frac{R_2}{R_1} \]

\[ R_2 = R_4 + R_3 \]

\[ R_1 = R_3 \]

Sample and Hold

*Polycarbonate-dielectric capacitor
Section 3 — Signal Processing (Continued)

Sample and Hold

![Sample and Hold Circuit Diagram]

*Worst case drift less than 2.5 mV/sec
†Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

Low Drift Integrator

![Low Drift Integrator Circuit Diagram]

*Q1 and Q3 should not have internal gate-protection diodes.
Worst case drift less than 500 µV/sec over −55°C to +125°C.
In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

† Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/µs

\[
\tau C5 = 6 \times 10^{-8} \frac{\text{Rf}}{\text{Ri}}
\]

Fast Integrator with Low Input Current
Section 3 — Signal Processing  (Continued)

Adjustable Q Notch Filter

\[ f_0 = \frac{1}{2\pi R_1 C_1} \]
\[ = 60 \text{ Hz} \]
\[ R_1 = R_2 = R_3 \]
\[ C_1 = C_2 = C_3 \]
Section 3 — Signal Processing (Continued)

Easily Tuned Notch Filter

![Circuit Diagram](image1)

\[ f_o = \frac{1}{2\pi R_4 C_1 C_2} \]

R4 = R5
R1 = R3
R4 = \frac{1}{2} R1

Tuned Circuit

![Circuit Diagram](image2)

\[ f_o = \frac{1}{2\pi R_1 R_2 C_1 C_2} \]

Two-Stage Tuned Circuit

![Circuit Diagram](image3)

\[ f_o = \frac{1}{2\pi R_1 R_2 C_1 C_2} \]
Section 3 — Signal Processing  (Continued)

**Negative Capacitance Multiplier**

\[ C = \frac{R_2}{R_3} C_1 \]

\[ I_L = \frac{V_{os} + R_2 I_{os}}{R_3} \]

\[ R_S = \frac{R_3(R_1 + R_{in})}{R_{in} A_{vo}} \]

**Variable Capacitance Multiplier**

\[ C = \left( 1 + \frac{R_b}{R_a} \right) C_1 \]
Simulated Inductor Capacitance Multiplier

\[ L \geq R_1 R_2 C_1 \]

[Equation]

\[ R_S = R_2 \]

[Resistance]

\[ R_P = R_1 \]

[Resistance]

High Pass Active Filter

\[ C = \frac{R_1 C_1}{R_2} \]

[Capacitance]

\[ I_L = \frac{V_{os} + I_{os} R_1}{R_3} \]

[Isoelectric Current]

\[ R_S = R_3 \]

[Resistance]

Low Pass Active Filter

*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.
Section 3 — Signal Processing  (Continued)

Nonlinear Operational Amplifier with Temperature Compensated Breakpoints

Current Monitor

\[ V_{\text{OUT}} = \frac{R_1 \cdot R_3}{R_2} \cdot I_L \]
Section 3 — Signal Processing (Continued)

Analog Multiplier

\[ R_5 = R_1 \left( \frac{V^-}{10} \right) \]
\[ V_1 \geq 0 \]
\[ V_{OUT} = \frac{V_1 V_2}{10} \]

Long Interval Timer

Fast Zero Crossing Detector

*Low leakage ~0.017 \( \mu F \) per second delay

Propagation delay approximately 200 ns

\^DTL or TTL fanout of three.

Minimize stray capacitance

Pin 8
Amplifier for Piezoelectric Transducer

Low frequency cutoff = R1 C1

Photodiode Amplifier

V_{OUT} = R1 I_D

Photodiode Amplifier

V_{OUT} = 10 \text{ V/\mu A}

High Input Impedance AC Follower

*Operating photodiode with less than 3 mV across it eliminates leakage currents.
Section 3 — Signal Processing

Temperature Compensated Logarithmic Converter

10 nA < I_{IN} < 1 mA
Sensitivity is 1V per decade
†1 kΩ (±1%) at 25°C, +3500 ppm/°C.
Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.
*Determines current for zero crossing on output: 10 µA as shown.

Root Extractor

*2N3728 matched pairs
Section 3 — Signal Processing (Continued)

Multiplier/Divider

$$E_{\text{OUT}} = \frac{E_1}{E_2}$$
for
$$E_1 \geq 0 \text{ and } E_2 \geq 0$$

Cube Generator
Section 3 — Signal Processing  (Continued)

Fast Log Generator

\[ E_{\text{REF}} \]

\[ 15V \]

\[ R_3 \]

\[ 150K \]

\[ 1\% \]

\[ 2 \]

\[ 3 \]

\[ R_5 \]

\[ 150K \]

\[ 1\% \]

\[ C_1 \]

\[ 300 \text{ pF} \]

\[ C_2 \]

\[ 75 \text{ pF} \]

\[ C_3 \]

\[ 1 \text{ pF} \]

\[ A_3 \]

\[ \text{LM102} \]

\[ 8 \]

\[ 6 \]

\[ R_6 \]

\[ 1K \]

\[ R_7 \]

\[ 1K \]

\[ \text{OFFSET ADJUST} \]

\[ V^* \]

\[ 6 \]

\[ 2 \]

\[ \text{2N2920} \]

\[ 1 \]

\[ 3 \]

\[ A_2 \]

\[ \text{LM101A} \]

\[ 8 \]

\[ 6 \]

\[ R_4 \]

\[ 2K \]

\[ C_4 \]

\[ 15 \text{ pF} \]

\[ C_5 \]

\[ 150 \text{ pF} \]

\[ \] 1 kΩ (±1%) at 25°C, +3500 ppm/°C.

Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

Anti-Log Generator

\[ E_{\text{REF}} \]

\[ 15V \]

\[ R_3 \]

\[ 150K \]

\[ 1\% \]

\[ 2 \]

\[ 3 \]

\[ R_5 \]

\[ 150K \]

\[ 1\% \]

\[ C_1 \]

\[ 150 \text{ pF} \]

\[ C_2 \]

\[ 20 \text{ pF} \]

\[ R_4 \]

\[ 2K \]

\[ A_1 \]

\[ \text{LM101A} \]

\[ 6 \]

\[ 2 \]

\[ \text{2N2920} \]

\[ 1 \]

\[ 3 \]

\[ A_2 \]

\[ \text{LM101A} \]

\[ 6 \]

\[ 2 \]

\[ C_4 \]

\[ 5 \text{ pF} \]

\[ C_3 \]

\[ 150 \text{ pF} \]

\[ \] 1 kΩ (±1%) at 25°C, +3500 ppm/°C.

Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.
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